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Application of nonlinear systems for designing low-power logic gates based on stochastic resonance

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Abstract: This paper presents a novel application of an operational transconductance amplifier configuration for implementing the basic logic gates using the concept of stochastic resonance (SR). In such framework, the SR effect applied to nonlinear electrical systems to build logical gates (SR gates) has been studied. The property of hysteresis is crucial: first, it reduces the error rate regarding mismatch problems with cooperative use of noise, and second, it ensures the stability of all logic states. However, in this configuration, the toggles exhibit an unpredictable delay, which has been reviewed in this study; therefore, the most suitable application of the SR gates is in asynchronous circuit design. Circuit performance was electrically simulated using SPICE for 0.18-μm CMOS technology. The simulation results have proven the effective performance of the SR gates for an optimal amount of noise working at low power consumption, despite the introduction of an intentional mismatch between the threshold voltages of the transistors.

Key Words: stochastic resonance, low power consumption, logic gates

1. Introduction

The use of an optimal amount of noise was proven to be an effective method to improve specific tasks. One of the most well-known effects is stochastic resonance (SR) [1, 2], and it is exhibited in several biological systems [3–5]. One of the main applications of the SR effect is for the improvement of the response in models based on threshold systems [6–9]. A novel application of the SR effect in nonlinear systems is in the field of digital circuit design [10], where a certain range of noise serves to change the state in a bistable system; each state represents a logic state, and therefore the basic logic operations can be implemented by electrically modeling a double-well potential function with an additive Gaussian noise [11]. Further, the precise values for the bias are necessary to set the logical operation, and this requires additional bias sources. Moreover, the implementation of this system is quite complex because it requires the use of several operational amplifiers and additional bias circuits, which is expensive in terms of VLSI.

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This paper proposes a novel configuration that utilizes the cooperative role of noise in nonlinear systems. The concept involves electrical systems that exhibit hysteresis characteristic. This can be achieved easily by using an operational transconductance amplifier with positive feedback [12]. In this case, the presence of two thresholds prevents the activation of the output in the presence of large noise fluctuations [13]. However, the main limitation is the timing of the SR gates, as discussed later. The delay time of the SR gate response is limited by the stochastic process; therefore, synchronization is the main limitation for the effective performance of high-complexity synchronous circuit configurations. However, a suitable alternative is the implementation of asynchronous circuits with the current SR gates, considering the lack of a common clock [14]. This characteristic allows for more reliable designs of the elements in the presence of delays, as in the SR gate.

The reminder of this paper is organized as follows. Section 2 provides a description of the main idea for designing the stochastic resonance logic gates. Section 3 presents electrical simulations and experimental results. Section 4 contains a brief discussion regarding future applications. Finally, Section 5 presents the summary of this work.

2. Electrical circuit design of the SR gates

Our idea is based on the utilization of noise to build logic gates. The main design is based on electrical systems with hysteresis characteristics, where the input is represented as a weighted sum of logic inputs (Fig. 1(a), rightmost subfigure). Traditionally, noise assistance has been used to improve subthreshold-signal detection in systems with one threshold. Here, the red dot represents the subthreshold signal (center-left subfigure); subthreshold signals can be driven by noise to higher values than the threshold θ (gray dot at center-right subfigure). However, one evident problem is that a high-amplitude peak in the noise signal can trigger an unnecessary response (rightmost subfigure). Generally, this response has hazards.

Figure 1(b) represents our approach, utilizing nonlinear systems with two thresholds: $\theta_{y^+ \to y^-}$ and $\theta_{y^- \to y^+}$ (center-left subfigure). The first one is defined as the necessary threshold to change from the positive state y^+ to the negative state y^-, and the second one, represents the necessary threshold to change from y^- to y^+. Due to this hysteresis characteristic the output will be stable (rightmost subfigure).

Figure 2 shows a subthreshold operational transconductance amplifier (OTA), where V_{g1} and V_{g2}

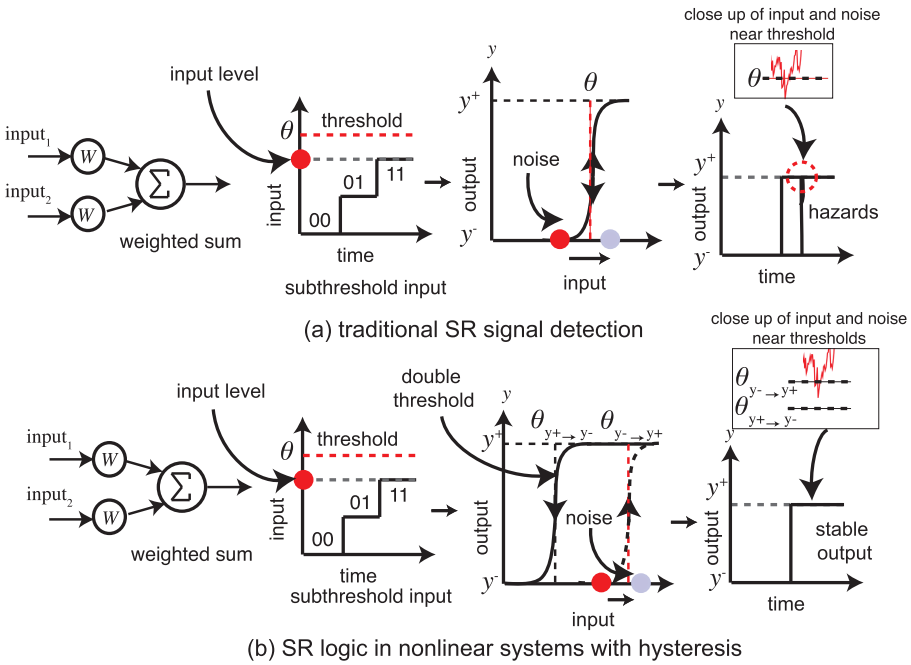


Fig. 1. (a) Noise assistance in nonlinear systems with one threshold; (b) noise assistance in nonlinear systems exhibiting hysteresis.

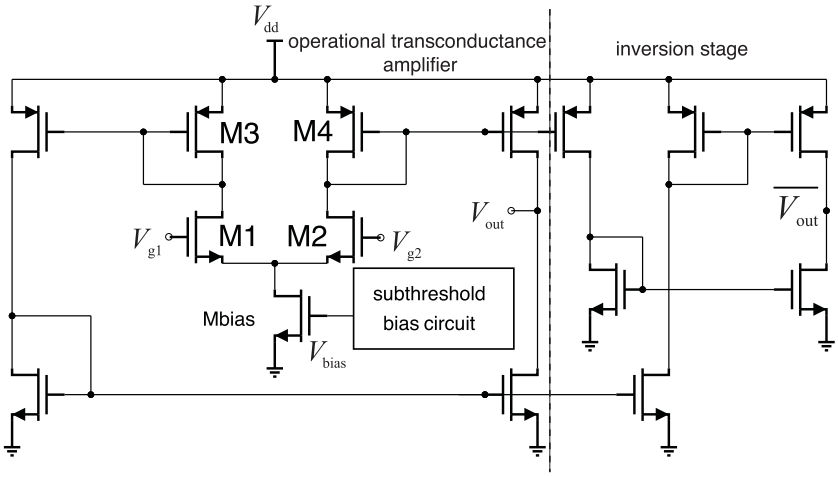


Fig. 2. CMOS design of the subthreshold operational transconductance amplifier (OTA).

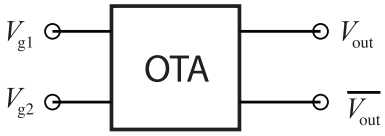


Fig. 3. Generic symbol of an OTA.

denote the input gate voltages, and V_{out} and $\overline{V_{\text{out}}}$ are the outputs. $\overline{V_{\text{out}}}$ is obtained by adding two current mirrors to invert the output. This is carried out in order to maintain a high-impedance node as in the non-inverted output V_{out}.

The generic symbol of the four-terminal OTA is shown in Fig. 3. Figure 4 shows the electrical connections of the generic SR gate for implementing the four basic logic operations. The inputs are capacitively coupled, where the values of V_{g1} and V_{g2} are the weighted sum of the input capacitors. This weighted sum is easily implemented with a floating-gate MOSFET (FGMOSFET) owing to its inherent property that generates a floating-gate potential equal to the weighted sum of its inputs [15].

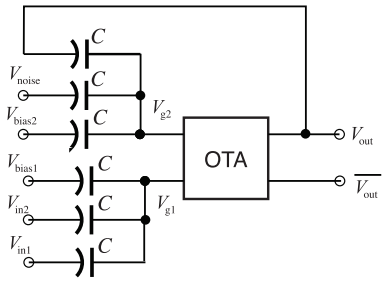


Fig. 4. Construction of the proposed SR gate configuration for the basic logic operations. The configuration depends on the values of V_{bias1} and V_{bias2}.

For Fig. 4, based on the equations of the FGMOSFET [15], the gate voltages V_{g1} and V_{g2} are given by Eq. (1) and Eq. (2) respectively:

$$V_{\text{g1}} = W(V_{\text{in1}} + V_{\text{in2}} + V_{\text{bias1}}) \tag{1}$$

$$V_{\text{g2}} = W(V_{\text{bias2}} + V_{\text{noise}} + V_{\text{out}}) \tag{2}$$

where W is a coupling factor and is defined as $W = C/C_{TOT}$, C is the input capacitor, and C_{TOT} is the total capacitance given by the sum of all input capacitances (excluding parasitic capacitances small enough to be neglected). To generate logic operations we used the concept of threshold logic. For example, if we consider a two input FGMOSFET, where input capacitors are equal, then each input is multiplied by a factor of 0.5. If each input is mapped as a logic input, then the input combinations

will be represented as a weighted sum. If there is at least a logic one , the weighted sum will be half of the total. If both inputs are logic one, then the weighted sum will be at its maximum value. Here, $V_{\rm bias1}$ and $V_{\rm bias2}$ serve as selectors for the logic operations. Table I lists the combinations of $V_{\rm bias1}$ and $V_{\rm bias2}$ to set either the NOR or NAND operation with $V_{\rm out}$ as the output. By selecting $\overline{V_{\rm out}}$ as the output, both the OR and AND operations can be performed.

Table I. Selection of the logic operations according to $V_{\rm bias1}$ and $V_{\rm bias2}$ as well as $V_{\rm out}$ and $\overline{V_{\rm out}}$.

$V_{\rm bias1}$	$V_{\rm bias2}$	$\overline{V_{\rm out}}$	$V_{\rm out}$
$V_{\rm dd}$	0 V	OR	NOR
$V_{\rm dd}$	$V_{\rm dd}$	AND	NAND

On the other hand, in order to confirm the operation of the SR gates, we show a suitable mathematical model for the SR logic gates based on the work of McNamara *et al.* [17]. For simplicity, we omitted the bias sources $V_{\rm bias1}$ and $V_{\rm bias2}$ in the analysis, since they serve only as threshold modifiers. Considering normalizing values of $+1$ and -1, for high logic and low logic respectively, the normalized output of the OTA can be given by:

$$y = sgn(z) \tag{3}$$

where $y = +1$ if $z > 0$, and $y = -1$ if $z < 0$. In this analysis, we consider a periodic signal as input $V_{\rm g1}$, where $V_{\rm in} = V_{\rm s}\cos\omega_{\rm s}t$, and $V_{\rm g2} = W(V_{\rm out} + V_{\rm noise})$. If we define the normalization factors as $\varepsilon = V_{\rm in}/V_{\rm dd}$ and $\sigma' = V_{\rm noise}/\gamma V_{\rm dd}$ ($V_{\rm dd}$ is the power supply), then Eq. (3) can be expressed as:

$$y = \mathrm{sgn}(\frac{\gamma}{2}(y+1) + \sigma'\xi(t) - \varepsilon) \tag{4}$$

where $\xi(t)$ represents white noise with a standard deviation σ'. The factor γ is defined as a normalized threshold that is directly proportional to W and it is related with other transistor parameters. In this system, a double threshold is generated due to the positive feedback of the OTA configuration. Considering Eq. (4) without noise, if $y = +1$, then $\varepsilon > \gamma$ is necessary to change state, therefore the threshold to change from positive to negative state is $\theta_{y^+\to y^-} = \gamma$. On the other hand , if $y = -1$, then $\varepsilon < 0$ is required to change y to the positive state, and the new threshold is given by $\theta_{y^-\to y+} = 0$. A realistic approximation to avoid infinite power is proposed by considering colored noise, where $\tau_{\rm c}$ is the correlation time, and the switching time should be short compared with $\tau_{\rm c}$. Therefore an approximate dynamical model of the OTA is given by:

$$\dot{y} = -\beta\{y - \tanh[A(\frac{\gamma}{2}(y+1) + x - \varepsilon)]\} \tag{5}$$

$$\dot{x} = -kx + \sigma\xi(t) \tag{6}$$

where noise is modeled as an Ornstein-Uhlenbeck process (Eq. (6)), where $k = \tau_c^{-1}$, and $\sigma = \sqrt{2k}\sigma'$. β^{-1} is the time constant. When β and $A \to \infty$, the behavior is approximated to an ideal OTA with positive feedback. This system has two stable states at y^+ and y^- in the range of $\varepsilon - \gamma < x < \varepsilon$. As we are interested in demonstrating the beneficial utilization of noise, equations for transition rate are analyzed. Let us define $x^- = \varepsilon - \gamma$ and $x^+ = \varepsilon$, where a transition from y^- to y^+ is given when $x > x^+$ and a transition from y^+ to y^- is given when $x < x^-$. The transition rate W_+ can be then obtained from the reciprocal of the mean passage time $T(x^- \to x^+)$. Defining $u = x\sqrt{k}/\sigma$, $u^- = x^-\sqrt{k}/\sigma$, and $u^+ = x^+\sqrt{k}/\sigma$, we have:

$$W_+^{-1}(x^- \to x^+) = \frac{2\sqrt{\pi}}{k}\int_{u^-}^{u^+} e^{u^2}\phi(u)du \tag{7}$$

where:

$$\phi(u) = \frac{1}{\sqrt{\pi}}\int_{\infty}^{u} e^{u^2}du \tag{8}$$

Executing numerical integrations, Eq. (7) and (8) were solved. The parameters for numerical simulations were set to $\varepsilon = 0.467$, $\gamma = 0.682$, and $\sigma = 0.07$. A qualitatively behavior was confirmed

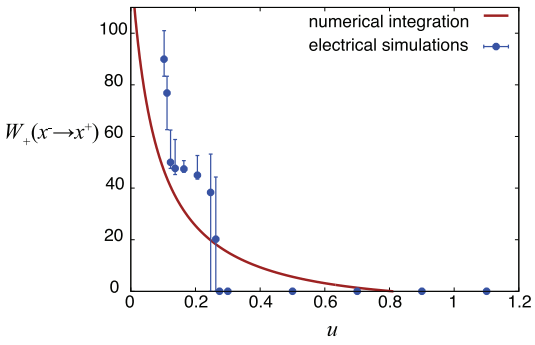


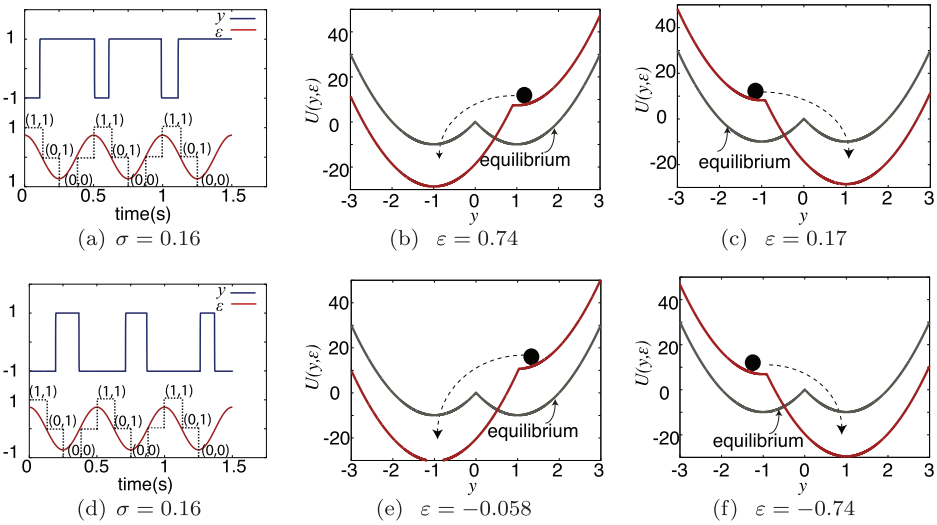
Fig. 5. Transition rate $W_+(x^- \to x^+)$.

(Fig. 5), notice that u is inversely proportional to σ, therefore as σ is increased, transition rate is increased exponentially, confirming the role of noise to generate a transition.

An equation for the potential function can be also obtained by integrating Eq. (4), and it is given by the following equation:

$$U(y,t) = \beta\{\frac{1}{2}y^2 - \frac{2}{\gamma A}\ln\cosh[A(\frac{\gamma}{2}(y+1) + x - \varepsilon + \alpha)]\} \tag{9}$$

here, α is the normalized value of a bias voltage V_{bias}, defined as $\alpha = V_{\text{bias}}/\gamma V_{\text{dd}}$. Figure 6 shows numerical simulations for the double-well potential, where α modifies the double-well potential to generate logic operations NAND and NOR. Here, $\sigma = 0.16$ and ε is represented as the weighted sum of two inputs: I_1 and I_2. These inputs can be mapped to the logic input sets: (0,0), (1,0), (0,1), and (1,1) (dashed stepwise graph at Fig. 6(a) and 6(d)).



(a) $\sigma = 0.16$ (b) $\varepsilon = 0.74$ (c) $\varepsilon = 0.17$

(d) $\sigma = 0.16$ (e) $\varepsilon = -0.058$ (f) $\varepsilon = -0.74$

Fig. 6. Figure 6(a) represents NAND operation, with a subthreshold input ε (red line) and output y (blue line), where $\gamma = 0.682$, $\alpha = 0.142$, and $\beta = 5x10^{-4}$. Figure 6(b) represents the double-well potential obtained from Eq. (9), when ε is near the threshold $\theta_{y^+ \to y^-}$, the transition probability increases. Figure 6(c) represents the opposite case for $\theta_{y^- \to y^+}$. To generate NOR operation, $\alpha = -0.77$ (Fig. 6(d)). Figure 6(e) and 6(f) are the double-well potential for the cases of ε near $\theta_{y^+ \to y^-}$ and $\theta_{y^- \to y^+}$ respectively.

3. Simulation and experimental results

This section is divided into two subsections: the first one discusses the simulations of the performance of the SR gates as well as the experimental results, and the second one details the results regarding the timing analysis of the SR gates.

3.1 Performance of the SR logic gates

The circuit simulations are carried out by using a SPICE program using 0.18-μm CMOS technology. The power supply is set to 0.35 V. This value corresponds to the minimum power supply for which the error rate of the SR gates is zero, considering a variation in $V_{\rm th}$ of M2 of 0.1 V, where $V_{\rm th}$ represents the transistor threshold voltage. All transistors operate in the subthreshold region. Gaussian noise is introduced in $V_{\rm noise}$ with a mean value of zero, a standard deviation $\sigma_{V_{\rm noise}}$ of 18 mV, and an offset voltage of $V_{\rm dd}$. This value was obtained through electrical simulations and corresponds to the value of the standard deviation of noise for which a circuit error rate of zero is achieved.

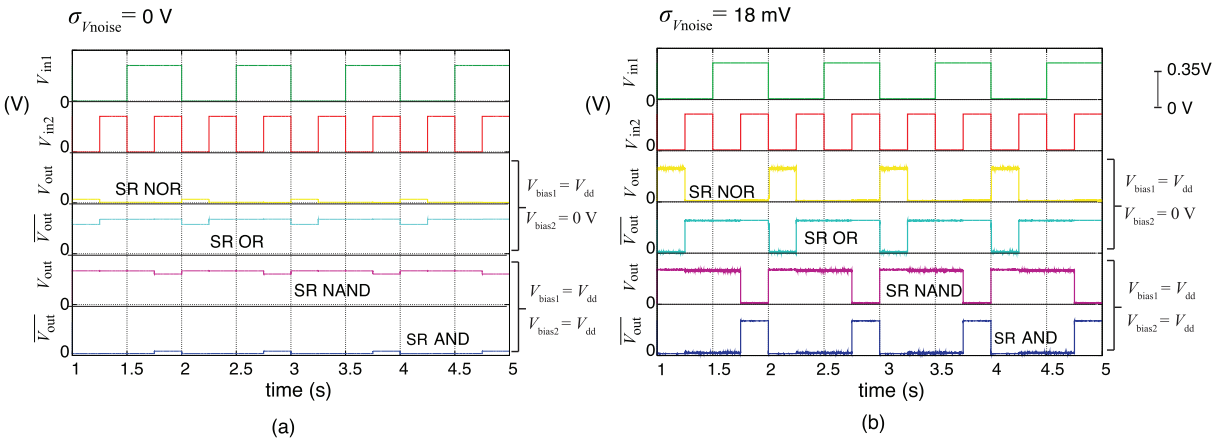


Fig. 7. Simulation results of an SR gate for NOR, OR, NAND and AND operations. (a) for $\sigma_{V_{\rm noise}} = 0$ V, the logic operations are not generated. (b) for $\sigma_{V_{\rm noise}} = 18$ mV, the logic operations are generated correctly.

The SR effect is observed during the simulations. For $\sigma_{V_{\rm noise}} = 0$ V, the inputs do not exceed the threshold, and there is no response (Fig. 7(a)). Figure 7(b) shows the simulation results of the SR gates of the four basic logic gates when $\sigma_{V_{\rm noise}} = 18$ mV. These responses are consistent with the true table of each logic gate, demonstrating that the application of noise helps to recover the logic operations in the presence of mismatches. It is also observed that the outputs exhibit low amplitude fluctuations that can be explained as a result of the direct application of noise to one of the floating gate inputs of the operational transconductance amplifier.

Moreover, three basic simulations were performed: the first one shows a SPICE simulation of the power consumption P versus the power supply $V_{\rm dd}$ and the standard deviation of $V_{\rm th}$ ($\sigma_{V_{\rm th}}$) (Fig. 8). This simulation was obtained by calculating the average current of $V_{\rm dd}$ using the control commands of the SPICE simulator. This graph shows that the average power performance is on the order of picowatts , which makes the SR logic gates suitable for low-power applications.

Electrical simulations were also performed to compare the power consumption of a conventional transistor-based NAND gate and our approach. Figure 9 shows that in the region where logic function is achieved correctly, the power consumption of the SR gates is lower, in the order of picowatts.

However, one implication of working with low power consumption is the increase in the sensitivity to variations in the threshold voltage, particularly in differential-pair configurations, where precise matching is required between the transistors. However, in this particular case, noise actually improves the performance regarding fluctuations in the threshold voltage, as shown in Fig. 10. This simulation consists of a phase diagram of the error rate versus two variables: $V_{\rm dd}$ and $\sigma_{V_{\rm th}}$. Here, intra-die variations are considered instead of the worst-case threshold-voltage variation. Monte Carlo simulations were carried out for ten values of $\sigma_{V_{\rm th}}$. Each one was set to six different values of $V_{\rm dd}$. The phase diagram shows the region where the error rate corresponds to 0%. The error rate greater than 0% is outside of this region.

Moreover, experimental results were performed by implementing a macrosystem for the SR NAND gate (Fig. 11). An operational amplifier OP284 was connected with positive feedback to generate the hysteresis characteristic.

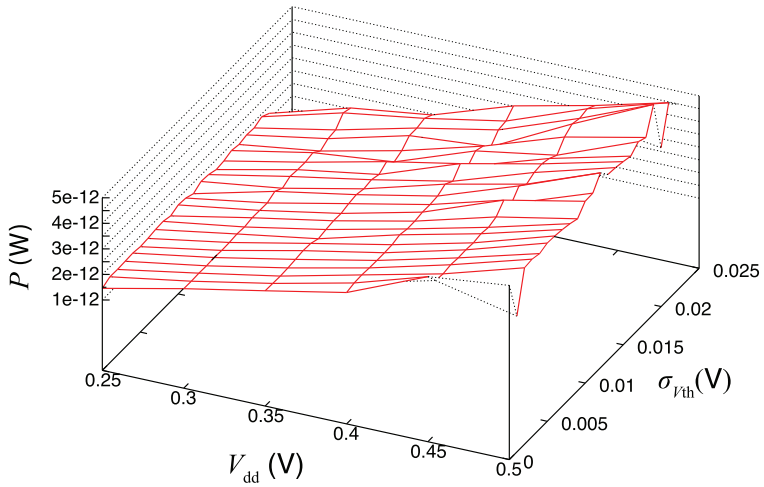


Fig. 8. Power consumption of the SR NAND gate versus V_{dd} and $\sigma_{V_{\mathrm{th}}}$.

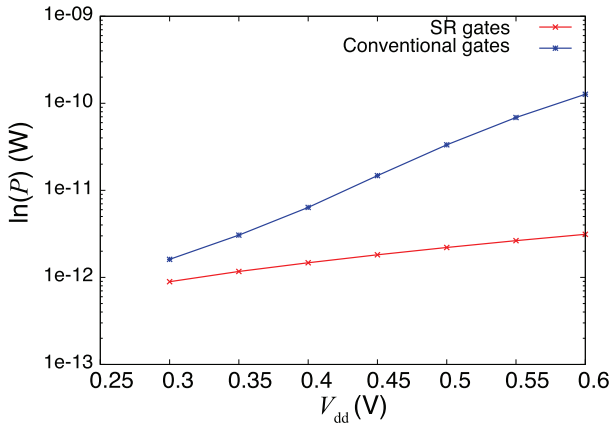


Fig. 9. Power consumption of a conventional NAND gate and a SR NAND gate.

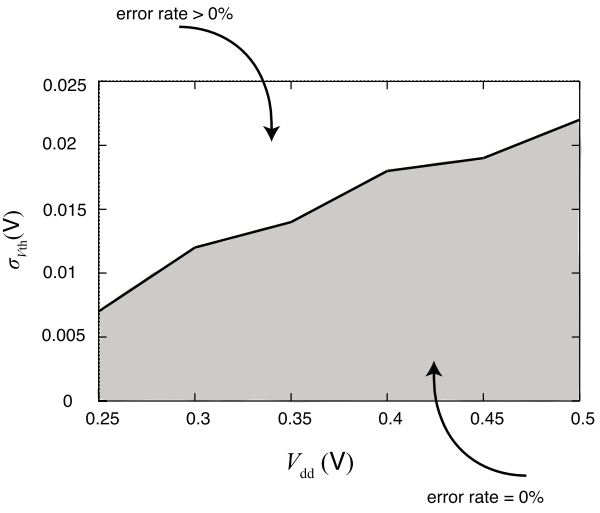


Fig. 10. Phase diagram of the SR NAND gate error rate versus V_{dd} and $\sigma_{V_{\mathrm{th}}}$.

The supply voltage was set to +1.5 V and −1.5 V. In the case of floating-gate technology, the gate potential is isolated electrically from the rest of the circuit. However, it is not possible to completely isolate the input of the operational amplifier. The digital inputs were connected through two resistors to emulate the weighted sum of the inputs of the FGMOSFET at the negative input of the operational amplifier [17]. To indirectly emulate fluctuations in threshold voltage, one of the digital inputs (V_{in1}) was set to $V_{\mathrm{pp}} = 1.5$ V, where V_{pp} is defined as the amplitude of the pulse, from −0.75 V to +0.75V;

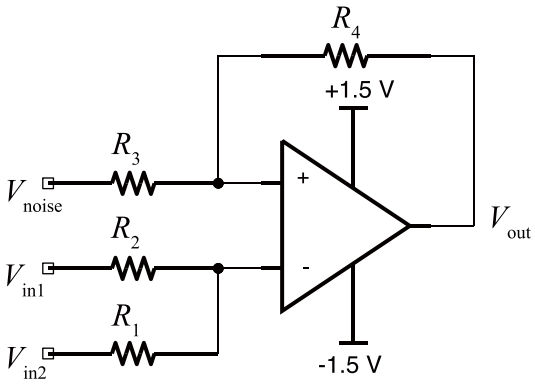


Fig. 11. OP284 with a positive feedback configuration.

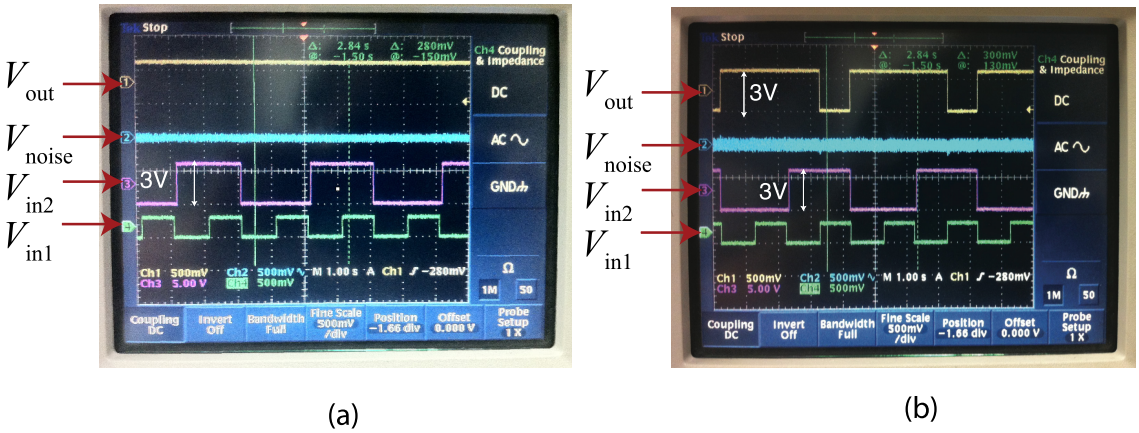


Fig. 12. Experimental results measured with a Tektronix TDS 3034 oscilloscope. (a) $\sigma_{V_{\mathrm{noise}}} = 100$ mV, low standard deviation of noise is not enough to detect the signal. (b) $\sigma_{V_{\mathrm{noise}}} = 150$ mV, the minimum standard deviation to effectively detect the signal, and generate the output corresponding to the NAND gate.

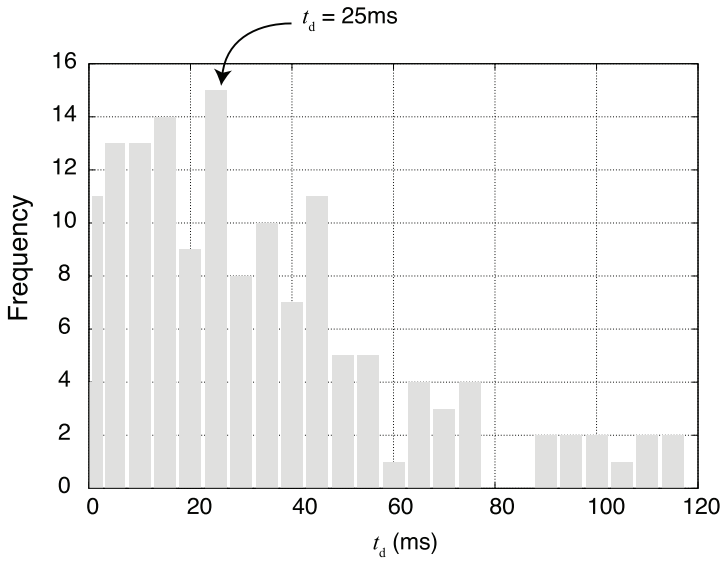


Fig. 13. Histogram for the delay time t_{d} of the response of the SR NAND gate.

while V_{in2} remained at $V_{\mathrm{pp}} = 3$ V. Noise was provided by the white noise source of an electrical waveform generator HIOKI 7075. First, no response is present without noise, but the circuit correctly generates the output of the SR NAND gate as the standard deviation of noise increases, as shown in Fig. 12.

3.2 Delay time of the SR logic gates

Owing to the stochastic nature of the SR logic, the response of the gates exhibits an unpredictable delay time. Figure 13 shows the frequency of the delay time t_d for intervals corresponding to 5 ms from 0 ms to 115 ms. These results correspond to the response of the SR NAND gate, where the time difference t_d between the input toggles and the output toggles was obtained.

Figure 13 shows that $t_d = 25$ ms is more likely to occur. The presence of t_d is critical for high-complexity synchronous digital circuits, where precise synchronization among digital blocks is required. Considering these results, the proper applications of the SR gates are in asynchronous circuit design.

4. C-element

Table II. C-element state table with input voltages mapped as logic inputs.

V_{in1}	V_{in2}	Y
0	0	0
0	1	Y^{-1}
1	0	Y^{-1}
1	1	1

As we mentioned previously, we proposed a suitable application in the field of asynchronous circuit design for the SR logic gates owing to the timing limitations. In the case of asynchronous circuit design, the performance of a circuit does not rely on a central clock but on handshaking protocols. Although there is not an established methodology for designing asynchronous logic, there are some basic digital circuits that are different from those in synchronous logic.

Therefore, there are some necessary configurations required to implement certain functions of the asynchronous logic in addition to the basic logic gates, as in the case of the C-element [18]. The C-element is a two-input gate, where the output stores the previous state Y^{-1} as long as both inputs

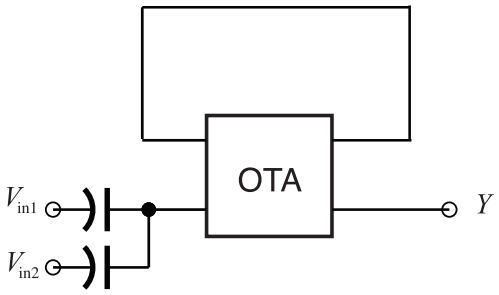


Fig. 14. Configuration for the C-element.

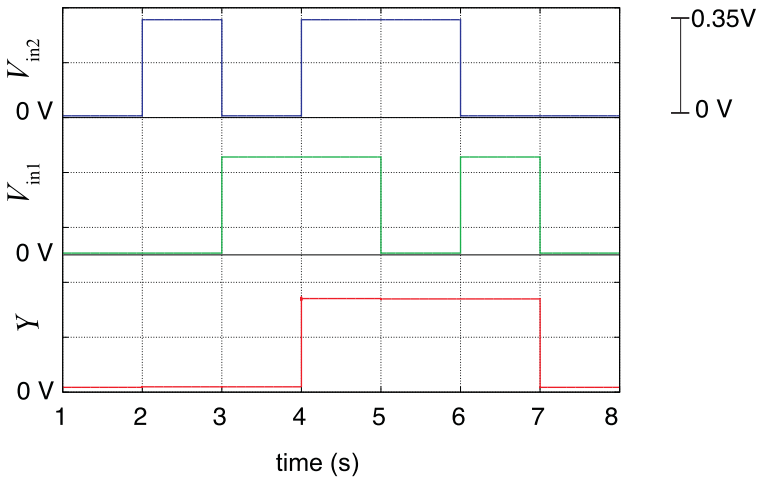


Fig. 15. Simulation results for the C-element.

are different (Table II). This configuration can be implemented as shown in Fig. 14 using the same OTA configuration. In this case, the feedback allows the previous state to be stored until both the inputs attain the same value. The simulation results are shown in Fig. 15 for a power supply of 0.35 V.

5. Discussion

As described in Sections 1 and 2, we proposed a novel configuration for noise-driven logic gates. In this approach, the hysteresis characteristic is necessary to overcome mismatch problems and to maintain the stability of the response. In addition, the selection of the logic operations is achieved by setting two external inputs. It should be noted that these values are set to either V_{dd} or zero, in comparison with previous works (as discussed in Section 1), where a precise V_{bias} value is required, and therefore, additional bias circuits must be implemented. Electrical simulations show the power consumption of the SR logic gates; these results demonstrate that the SR logic gates are suitable for applications in which low power consumption is required. Further, we conducted Monte Carlo simulations to measure the error rate versus the standard deviation of the threshold voltage. In this simulation, the area that represents an error rate of zero is increased in the presence of noise. This shows the ability of noise-driven responses for improving the circuit performance in the presence of threshold-voltage fluctuations. However, there is a delay time associated with the response of the SR gates. This characteristic directs the applications of SR logic gates to the field of asynchronous circuit design rather than synchronous circuit design, where precise synchronization is required. In this framework, we proposed the basis for asynchronous circuit design based on the SR logic gates. As the previous statistical simulation shows, this delay time has a mean value. Although this result may direct asynchronous circuit design on the basis of the worst-case approach for the delay time, it also requires a precise timing analysis, not only for a single logic gate, but for the entire circuit. This approach also requires the implementation of delay elements to synchronize control signals with data. A second approach assumes the design of delay-insensitive asynchronous circuits. These circuits are correct by design, and it is not necessary to add delay elements. This approach is the most suitable model for implementing our current work. The first step is to propose a configuration for one of the basic blocks of delay-insensitive asynchronous circuit design : the C-element. This element plays a key role in controlling the synchronization of several inputs arriving at different times owing to delays in their response. Our future work includes the design of asynchronous logic circuits using the proposed SR logic gates in combination with the C-element.

6. Summary

The SR effect has been demonstrated to be an effective technique to detect weak stimuli in nonlinear systems. The main contribution of this study is the use the hysteresis characteristic in a differential-pair configuration to avoid spontaneous hazards and high-amplitude oscillations. Owing to the fact that all transistors operate in the subthreshold regime, the circuit achieves low power consumption. According to the electrical simulations, power consumption is on the order of picowatts. In addition, the introduction of noise actually reduces the mismatch effect, which is more evident in subthreshold systems. The circuit simulations have demonstrated the effectiveness of using noise in the proposed configuration to build logical circuits. However, one of the limitations of these noise-driven logic gates is the timing response. Owing to the stochastic nature of this circuit, there is an unpredictable delay time. This drawback is critical for the correct performance of synchronous digital circuits, where precise synchronization among gates is required. In this regard, the most suitable application for these SR gates is asynchronous logic design. In our future work, we will study the design of high-level asynchronous circuit designs based on the SR logic.

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