LETTER *Special Section on VLSI Design and CAD Algorithms*

Low-Voltage Process-Compensated VCO with On-Chip Process Monitoring and Body-Biasing Circuit Techniques

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SUMMARY A voltage-controlled oscillator (VCO) tolerant to process variations at lower supply voltage was proposed. The circuit consists of an on-chip threshold-voltage-monitoring circuit, a current-source circuit, a body- biasing control circuit, and the delay cells of the VCO. Because variations in low-voltage VCO frequency are mainly determined by that of the current in delay cells, a current-compensation technique was adopted by using an on-chip threshold-voltage-monitoring circuit and body-biasing circuit techniques. Monte Carlo SPICE simulations demonstrated that variations in the oscillation frequency by using the proposed techniques were able to be suppressed about 65% at a 1-V supply voltage, compared to frequencies with and without the techniques.

key words: *voltage-controlled oscillator, process variation, process compensation, body bias, current reference*

1. Introduction

The power-supply voltage of LSI systems has been gradually decreasing with progress in CMOS-device technology. Their power supply has become approximately twice the threshold voltage of MOSFETs. In advanced technology, MOSFETs are operated at near the threshold-voltage region. Although reducing the power supply achieves low-power dissipation, it also causes unwanted effects, i.e., threshold-voltage variations, in circuit systems operating at lower power-supply voltages.

Ring-oscillator-based voltage-controlled oscillators (VCOs) are the building blocks of such systems and are widely used in various CMOS LSI applications, e.g., phase locked loops (PLLs), frequency synthesizers, and clock data-recovery circuits. As previous described, the clock frequency of VCOs operating at near the threshold-voltage region changes significantly with threshold-voltage variations. For example, VCO in PLL has to be capable of a wide tuning range. However, the tuning range will be shifted or reduced by the variation of performance in VCO. Therefore, a method of design that provides sufficient performance in circuits even at lower supply voltages is required.

In this paper, a low-voltage process-compensated VCO is proposed. Because variations in clock frequency are caused by operation current in the delay cells of VCOs, current-compensation techniques were adopted by using an on-chip threshold-voltage-monitoring circuit and body-biasing circuit techniques. A reference current generated by using an on-chip threshold-voltage-monitoring circuit and a current-source circuit controls the body-bias voltage of MOS transistors so that the operation current in the VCO is equal to the reference current. The clock frequency variations in the VCO due to threshold-voltage variations can be suppressed by using the techniques we propose. The following sections describe the VCO in detail.

Note that, all the simulations in this work were performed using a SPICE, SPECTRE level 53-model, and the parameter set of a 0.35-μm 2P4M-standard CMOS process, and that typical threshold voltages of a nMOSFET and pMOSFET corresponded to 0.52 V and 0.72 V, respectively.

2. Proposed VCO

A compact VCO only consisting of MOSFETs was proposed by Park and Kim [1] as shown in Fig. 1(A). However, the clock frequency of an VCO operating at a lower supply voltage changes significantly because operation current in delay cells changes with process variations. To solve this problem, current in delay cells is compensated for by using the proposed techniques. Figure 1(B) shows a circuit diagram of the proposed low-voltage process-compensated VCO. The circuit consists of a threshold-voltage-monitoring circuit [2], a current source circuit [3], a body-biasing control circuit, and the delay cells of the VCO [1]. The circuit operates as follows.

The threshold-voltage-monitoring circuit generates the threshold voltage of a MOSFET at 0 K (V_{TH0}), which has a linear dependence on die-to-die (D2D) threshold-voltage variation [2]. By using the output voltage as a bias voltage for an output transistor Mn in the current source circuit, a reference current I_{REF} that is independent of threshold voltage variations can be obtained [3]. To reduce within-die (WID) variation of the reference current I_{REF}, large-sized output transistor was used ($W/L = 4\,\mu\text{m}/5\,\mu\text{m}$). The body-biasing control circuit consists of a replica transistor Mp for a delay cell in the VCO, current mirrors, and a voltage buffer. The current-source circuit, replica transistor Mp, and current mirrors form a feedback loop through body-bias V_{COMP}. The circuit accepts reference current I_{REF} and generates appropriate body-bias-voltage V_{COMP} such that the current in a delay cell is equal to the reference current. The D2D threshold-voltage variations of the pMOSFET in the delay cells are compensated for so that the on-current of de-

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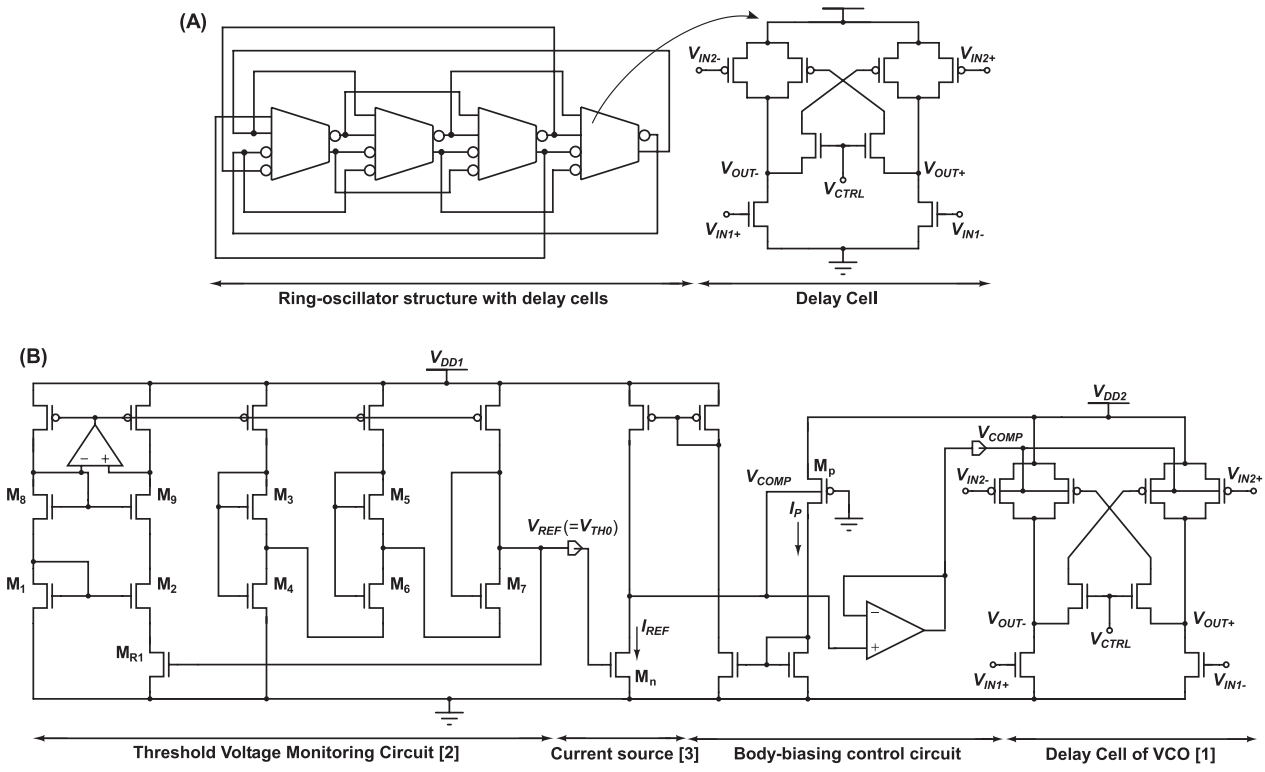

Fig. 1 Schematic of (A) ring-oscillator-based voltage-controlled oscillator reported in [1] and (B) proposed low-voltage process-compensated VCO.

lay cells is equal to the reference current that is independent of the D2D process variations. This way the current in the pMOSFETs in the VCO is maintained at reference current I_{REF}, and the oscillation frequency is independent of process variations.

Note that, because the threshold voltage of a pMOSFET is substantially larger than that of an nMOSFET in the process we used, the variations in threshold voltage in the pMOSFET have a significant impact on circuit performance. Therefore, the circuit compensates for process variations in pMOSFETs in this design.

3. Results

We confirmed the operation of the circuit with the aid of a SPICE simulation. The supply voltage V_{DD1} was set to 3 V, and V_{DD2} was swept in a range from 1 to 3 V. The VCO consisted of four-stage delay cells with a ring-oscillator structure [1]. The control voltage V_{CTRL} of the delay cell was set to 1 V. To verify the stability of the circuit operation with process variations, Monte Carlo simulations assuming both D2D variations (the parameters were varied with a uniform distribution: e.g., $-0.1\,\mathrm{V} < \Delta V_{TH} < 0.1\,\mathrm{V}$) and WID mismatch variations (the parameters were varied with a Gaussian distribution: e.g., $\sigma_{V_{TH}} = A_{V_{TH}}/\sqrt{LW}$) in all MOSFETs were performed by using the parameters provided by the manufacturer [4], [5].

The results for 200 runs are shown in Figs. 2(A) and (B). Figure 2(A) shows scatter plot of the output voltage V_{REF} as a function of D2D threshold voltage variation ΔV_{TH}. Each open circle shows V_{REF} for a run. Because the threshold-voltage-monitoring circuit generates the output voltage equal to the 0-K threshold voltage of MOSFETs, the value of V_{REF} depends linearly on ΔV_{TH} ($\Delta V_{REF}/\Delta V_{TH} \approx 1$). Figure 2(B) shows the distribution of I_{REF}. The average of I_{REF} was $5.2\,\mu$A, and the standard deviation was $0.4\,\mu$A. The process sensitivities (σ/μ: μ and σ are the mean value and the standard deviation of the distribution, respectively.) were 7.6%, including both D2D and WID variations. This is because the output voltage of the threshold-voltage-monitoring circuit changes with the variation of threshold voltage as shown in Fig. 2(A) and the voltage cancels the

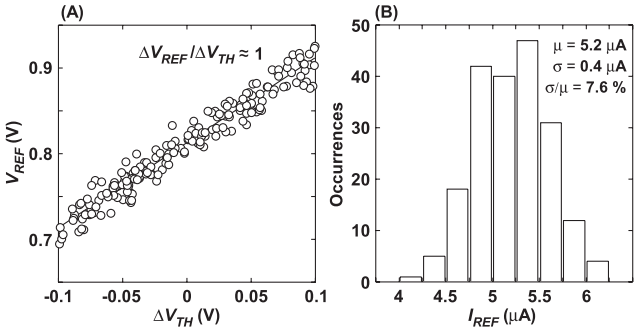

Fig. 2 (A) Scatter plot of the output voltage as a function of D2D threshold voltage variation. (B) Distribution of reference current from 200-point Monte Carlo simulations including D2D and WID variations.

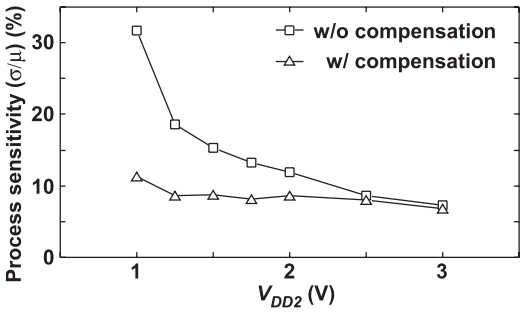

Fig. 3 Process sensitivity (σ/μ) of frequency in VCO with and without compensation circuit as a function of power supply.

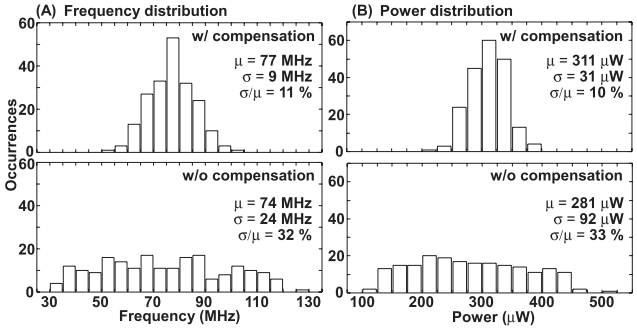

Fig. 4 Distribution of (A) frequency and (B) power dissipation of VCO with and without compensation circuit, and with 1-V control voltage (V_{CTRL}).

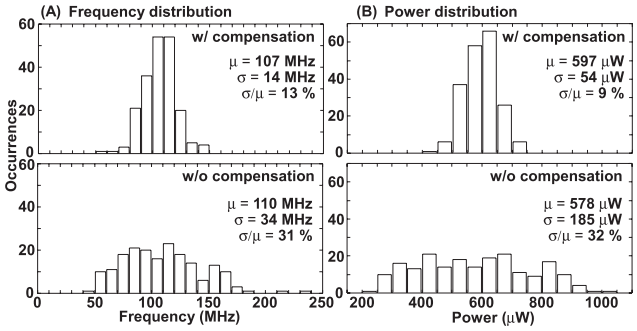

Fig. 5 Distribution of (A) frequency and (B) power dissipation of VCO with and without compensation circuit, and with 0-V control voltage (V_{CTRL}).

variation of the threshold voltage in transistor Mn.

Figure 3 shows the process sensitivities (σ/μ) of the oscillation frequency as a function of the supply voltage V_{DD2}. By using the compensation circuit, frequency variations with less than a 2-V power supply were able to be drastically suppressed. Figures 4 and 5 show the distribution of (A) oscillation frequency and (B) power dissipation, with 0-V and 1-V control voltage (V_{CTRL}), respectively. The supply voltage V_{DD1} and V_{DD2} were set to 2 V and 1 V, respectively. The power dissipation of the compensation circuits (a threshold-voltage-monitoring circuit, a current source, and a body-biasing control circuit) was 40 μW at room temperature. The process sensitivities (σ/μ) of both results with and without compensation were improved to about 65% by using the proposed circuit.

4. Conclusion

We proposed the process compensation techniques of VCO with on-chip process monitoring and body biasing circuits. The effect of process variations in VCO frequency can be significantly compensated for by applying this on-chip process compensation technique. The proposed technique will be useful for on-chip process compensation, because it can be applied without modifying the VCO circuit configuration.

Acknowledgments

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